EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

PHENIX LONGHORN, LCC, *Plaintiff,* v. WISTRON CORPORATION, *Defendant.*	§ § § § § § § §	Case No. 2:17-cv-00711-RWS (LEAD CASE) **JURY TRIAL DEMANDED**
PHENIX LONGHORN, LCC, *Plaintiff,* v. TEXAS INSTRUMENTS, INC., *Defendant.*	§ § § § § § § §	Case No. 2:18-cv-00020-RWS (CONSOLIDATED CASE) **JURY TRIAL DEMANDED**

CLAIM CONSTRUCTION
MEMORANDUM AND ORDER

Before the Court is Plaintiff Phenix Longhorn, LLC's opening claim construction brief (Docket No. 100), Defendants Texas Instruments and Wistron Corporation's joint response (Docket No. 104) and Plaintiff's reply (Docket No. 106). The Court held a hearing to determine the proper construction of the disputed claim terms in the U.S. Patent No. 7,233,305 (the " '305 Patent"). Docket No. 123. Based on the intrinsic and extrinsic evidence, the Court construes the

disputed terms in this Memorandum and Order. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 135 S. Ct. 831 (2015).

BACKGROUND

Phenix Longhorn, LLC ("Phenix") asserts the '305 Patent against Wistron Corporation and Texas Instruments, Inc. ("TI") (collectively, "Defendants"). The asserted claims are independent claim 1 and dependent claims 2, 4 and 5. The '305 Patent was previously asserted in *Phenix, LLC v. Integrated Memory Logic, Ltd.*, et al., No. 6:15-cv-00436-JRG-KNM ("*IML*"); however, that case settled prior to the court reaching a ruling on claim construction.

The '305 Patent relates generally to techniques to adjust the brightness of pixels of a liquid crystal display ("LCD"). The '305 Patent discloses a circuit and method for generating reference voltages to be used in such displays. More particularly, the '305 Patent describes using sets of gamma correction reference voltage to provide correction curves for correcting display characteristics. '305 Patent at 1:10–27. The Abstract of the '305 Patent recites:

> A programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in LCD displays. Once programmed, the buffers will continuously output the programmed value. The device incorporates a programming interface to allow the programming of the buffer outputs to the desired values during manufacturing and test of the panel. Multiple sets of values can be programmed to provide different gamma correction curves for different user or application requirements.

Id. at Abstract.

Figure 1 of the '305 Patent shows a prior art "diagram illustrating a conventional gamma reference circuit" in which resistors are used to fine-tune the reference voltages. *Id.* at 1:28–31, 1:46–47.

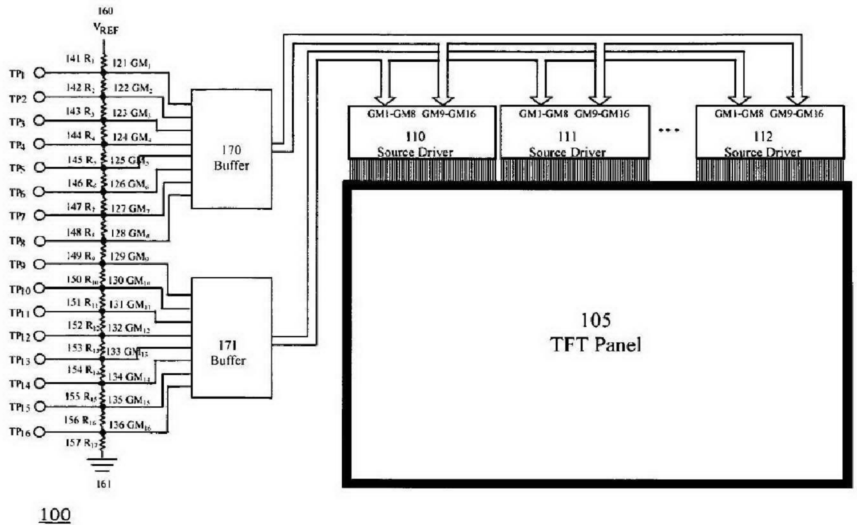


FIG. 1 -- Prior Art --

Id. at Figure 1. The '305 Patent describes the prior art approaches as too costly, too complex or not easily changeable due to being non-programmable. *Id.* at 1:31–2:10. The '305 Patent distinguishes its invention from the prior art as being programmable such that the output set of gamma correction reference voltages may be programed. *Id.* at Abstract, 2:15–20. The programmed value may be stored in non-volatile, programmable memory that maintains the programmed value even if power is removed. *Id.* at 2:19–22. Figure 2 illustrates an embodiment in which the circuitry is formed in first gamma reference controller 210, second gamma reference controller 220 and programming interface 230.

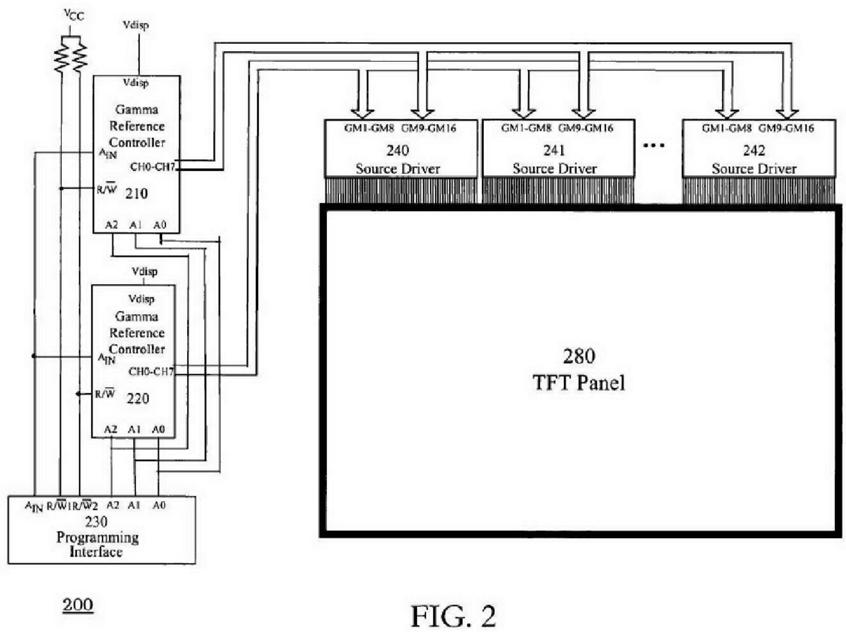


FIG. 2

Id. at Figure 2. A block diagram of a gamma reference controller is provided in Figure 3. As shown in Figure 3, elements 330–337 are programmable analog floating gate memory cells.

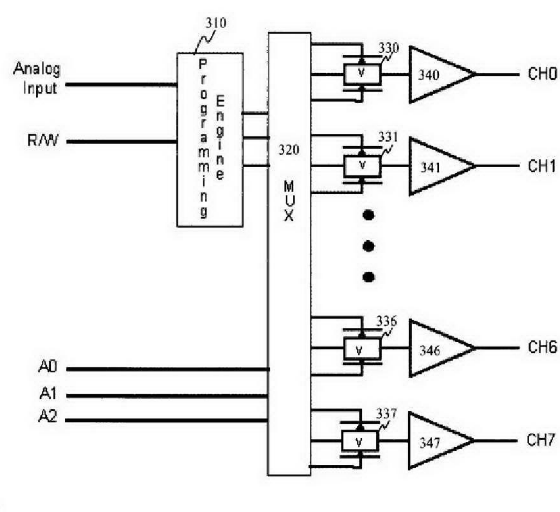


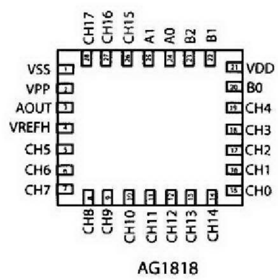
FIG. 3

Id. at Figure 3. The memory cells may be programmed to provide the desired correction reference voltages to the LCD display. *Id.* at 3:48–4:21. Different sets of reference voltage values may be

programmed for particular applications. *Id.* at 7:20–32. In one embodiment, the programmable gamma reference generator may be implemented in one integrated circuit (AG1818) as shown in Figure 4B.

FIG. 4B

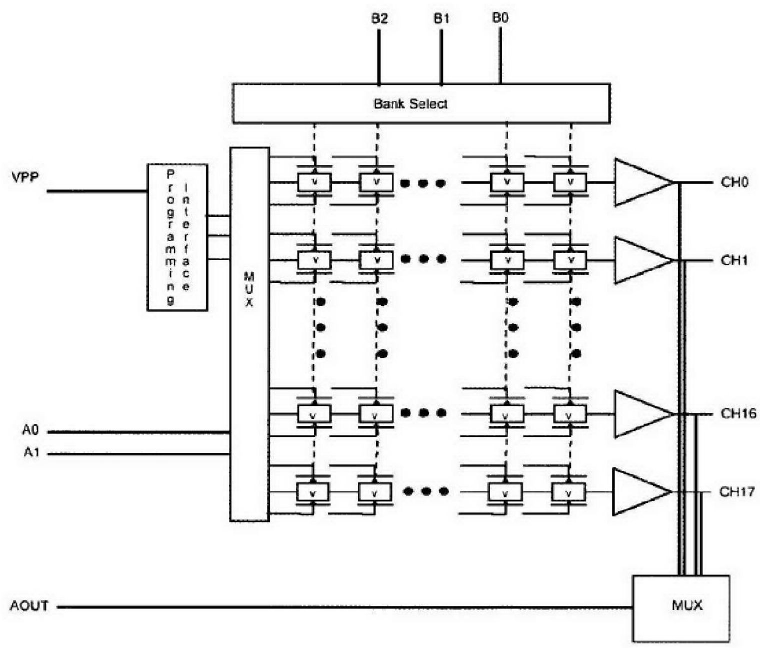
Pinout



Id. at Figure 4B. The integrated circuit is capable of storing eight independent groups of reference voltages, which may be stored in different banks of memory so that different gamma correction settings can be stored for different dynamic or application specific corrections. *Id.* at 5:50–59. Figure 6 provides a block diagram of the AG1818 integrated circuit.

FIG. 6

BLOCK DIAGRAM (AG1818)



Id. at Figure 6.

LEGAL PRINCIPLES

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.' " *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To determine the meaning of the claims, courts start by considering the intrinsic evidence. *Id.* at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004); *Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc.*, 262 F.3d 1258, 1267 (Fed. Cir. 2001). The intrinsic evidence includes the claims themselves, the specification and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. The general rule—subject to certain specific exceptions discussed *infra*—is that each claim

term is construed according to its ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the patent. *Phillips*, 415 F.3d at 1312–13; *Alloc, Inc. v. Int'l Trade Comm'n*, 342 F.3d 1361, 1368 (Fed. Cir. 2003).

"The claim construction inquiry . . . begins and ends in all cases with the actual words of the claim." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1248 (Fed. Cir. 1998). "[I]n all aspects of claim construction, 'the name of the game is the claim.' " *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1298 (Fed. Cir. 2014) (quoting *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998)). A term's context in the asserted claim can be instructive. *Phillips*, 415 F.3d at 1314. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id.* Differences among the claim terms can also assist in understanding a term's meaning. *Id.* For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id.* at 1314–15.

"[C]laims 'must be read in view of the specification, of which they are a part.' " *Id.* (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.' " *Id.* (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)); *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325 (Fed. Cir. 2002). But, " '[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the claims.' " *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1187 (Fed. Cir. 1998) (quoting *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988)); *see also Phillips*, 415 F.3d at 1323. "[I]t is

improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

The prosecution history is another tool to supply the proper context for claim construction because, like the specification, the prosecution history provides evidence of how the U.S. Patent and Trademark Office ("PTO") and the inventor understood the patent. *Phillips*, 415 F.3d at 1317. However, "because the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1318; *see also Athletic Alternatives, Inc. v. Prince Mfg.*, 73 F.3d 1573, 1580 (Fed. Cir. 1996) (ambiguous prosecution history may be "unhelpful as an interpretive resource").

Although extrinsic evidence can also be useful, it is " 'less significant than the intrinsic record in determining the legally operative meaning of claim language.' " *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc.*, 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id.* at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition are entirely unhelpful to a court. *Id.* Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read

claim terms." *Id.* The Supreme Court explained the role of extrinsic evidence in claim construction:

> In some cases, however, the district court will need to look beyond the patent's intrinsic evidence and to consult extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period. *See, e.g.*, *Seymour v. Osborne*, 11 Wall. 516, 546 (1871) (a patent may be "so interspersed with technical terms and terms of art that the testimony of scientific witnesses is indispensable to a correct understanding of its meaning"). In cases where those subsidiary facts are in dispute, courts will need to make subsidiary factual findings about that extrinsic evidence. These are the "evidentiary underpinnings" of claim construction that we discussed in *Markman*, and this subsidiary fact finding must be reviewed for clear error on appeal.

Teva Pharm. USA, Inc. v. Sandoz, Inc., 135 S. Ct. 831, 841 (2015).

A. Departing from the Ordinary Meaning of a Claim Term

There are "only two exceptions to [the] general rule" that claim terms are construed according to their plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution."[1] *Golden Bridge Tech., Inc. v. Apple Inc.*, 758 F.3d 1362, 1365 (Fed. Cir. 2014) (quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012)); *see also GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014) ("[T]he specification and prosecution history only compel departure from the plain meaning in two instances: lexicography and disavowal."). The standards for finding lexicography or disavowal are "exacting." *GE Lighting Solutions*, 750 F.3d at 1309.

To act as his own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term," and "clearly express an intent to define the term." *Id.* (quoting *Thorner*, 669

[1] Some cases have characterized other principles of claim construction as "exceptions" to the general rule, such as the statutory requirement that a means-plus-function term is construed to cover the corresponding structure disclosed in the specification. *See, e.g.*, *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1367 (Fed. Cir. 2002).

F.3d at 1365); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249.

To disavow or disclaim the full scope of a claim term, the patentee's statements in the specification or prosecution history must amount to a "clear and unmistakable" surrender. *Cordis Corp. v. Boston Sci. Corp.*, 561 F.3d 1319, 1329 (Fed. Cir. 2009); *see also Thorner*, 669 F.3d at 1366 ("The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope."). "Where an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

B. Functional Claiming and 35 U.S.C. § 112 ¶ 6 (pre-AIA) / § 112(f) (AIA)[2]

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112 ¶ 6; *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Section 112 ¶ 6 provides that a structure may be claimed as a "means . . . for performing a specified function" and that an act may be claimed as a "step for performing a specified function." *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002).

But §112 ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112 ¶ 6 applies when the claim language includes "means" or "step for" terms, and that it does not apply in the absence of those terms. *Masco Corp.*, 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. The presumption stands or falls according to whether one of ordinary skill in the art would understand the claim with the functional language, in the context of the entire specification, to denote sufficiently definite structure or acts for performing the function.

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[2] Because the application resulting in the '305 Patent was filed before September 16, 2012, the effective date of the AIA, the Court refers to the pre-AIA version of § 112.

See Media Rights Techs., Inc. v. Capital One Fin. Corp., 800 F.3d 1366, 1372 (Fed. Cir. 2015) (§ 112 ¶ 6 does not apply when "the claim language, read in light of the specification, recites sufficiently definite structure" (citing *Williamson*, 792 F.3d at 1349; *Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014))); *Williamson*, 792 F.3d at 1349 (section 112 ¶ 6 does not apply when "the words of the claim are understood by persons of ordinary skill in the art to have sufficiently definite meaning as the name for structure"); *Masco Corp.*, 303 F.3d at 1326 (section 112 ¶ 6 does not apply when the claim includes an "act" corresponding to "how the function is performed"); *Personalized Media Communications, L.L.C. v. International Trade Commission*, 161 F.3d 696, 704 (Fed. Cir. 1998) (section 112 ¶ 6 does not apply when the claim includes "sufficient structure, material, or acts within the claim itself to perform entirely the recited function . . . even if the claim uses the term 'means.' " (internal citation omitted)).

When it applies, § 112 ¶ 6 limits the scope of the functional term "to only the structure, materials or acts described in the specification as corresponding to the claimed function and equivalents thereof." *Williamson*, 792 F.3d at 1347. Construing a means-plus-function limitation involves multiple steps. "The first step . . . is a determination of the function of the means-plus-function limitation." *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). "[T]he next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id.* A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* The focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id.* The corresponding structure "must include all structure that actually performs the recited

function." *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). However, § 112 does not permit "incorporation of structure from the written description beyond that necessary to perform the claimed function." *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

For § 112 ¶ 6 limitations implemented by a programmed general purpose computer or microprocessor, the corresponding structure described in the patent specification must include an algorithm for performing the function. *WMS Gaming Inc. v. Int'l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999). The corresponding structure is not a general purpose computer but rather the special purpose computer programmed to perform the disclosed algorithm. *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

C. Definiteness Under 35 U.S.C. § 112 ¶ 2 (pre-AIA) / § 112(b) (AIA)[3]

Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112 ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). If it does not, the claim does not satisfy § 112 ¶ 2 and is therefore invalid as indefinite. *Id.* at 2124. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application for the patent was filed. *Id.* at 2130. As it is a challenge to the validity of a patent, the failure of any claim in suit to comply with § 112 must be shown by clear and convincing evidence. *Id.* at 2130 n.10. "[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012).

[3] Because the application resulting in the '305 Patent was filed before September 16, 2012, the effective date of the AIA, the Court refers to the pre-AIA version of § 112.

In the context of a claim governed by 35 U.S.C. § 112 ¶ 6, the claim is invalid as indefinite if the claim fails to disclose adequate corresponding structure to perform the claimed functions. *Williamson*, 792 F.3d at 1351–52. The disclosure is inadequate when one of ordinary skill in the art "would be unable to recognize the structure in the specification and associate it with the corresponding function in the claim." *Id.* at 1352.

AGREED TERMS

At the hearing, the parties agreed to the construction for the "multiplexer" term.

Term	Agreed Construction
multiplexer (claim 1)	one or more circuits that couple (1) one input (or one set of inputs) to one of many outputs (or one set of many sets of outputs) or (2) one of many inputs (or one set of many sets of inputs) to one output (or one set of outputs)

Docket No. 123 at 99–100.

DISPUTED TERMS

1. The Preamble of Claim 1 ("An integrated circuit for producing voltage signals on a plurality of outputs comprising:")

Phenix	Wistron	TI
The preamble of Claim 1 is a limitation reciting one integrated circuit	No construction needed / not limiting	Agrees with Phenix

Wistron contends that the preamble is not a limitation while Phenix and TI contend the preamble is a limitation that limits the claim to a single integrated circuit.

Positions of the Parties

Phenix first notes the basic preamble law: a preamble is a limitation "if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002). Phenix notes that the term "said integrated circuit" is also found at the end of claim 1 and that the specification

described "the invention" as being an integrated circuit. Docket No. 100 at 10–11 (citing '305 Patent at 7:60–61). Phenix further contends that the specification distinguished the invention from multi-component solutions, quoting the specification as follows: "the present invention advantageously allows a stand-alone solution such that it is not necessary to incorporate a micro controller unit (MCU)." '305 Patent at 2:33–35. Phenix also points to the examiner's statements in the Notice of Allowability as repeatedly referencing an integrated circuit. Docket No. 100 at 14. Phenix further notes that the experts of both Phenix and Wistron agreed that the ordinary meaning of "integrated circuit" refers to a single semiconductor chip. *Id.* at 15.

Wistron quotes the well-understood principle that "[g]enerally, the preamble does not limit claims." *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002). Wistron contends that the preamble here does not give "life, meaning, and vitality to the claim" and does not include any essential component of the invention. Docket No. 104 at 4.

Wistron responds that even when a preamble claim term is found in the body, that does not necessarily mean the preamble is always limiting. *Id.* at 5 (citing *Am. Med. Sys., Inc. v. Biolitec, Inc.*, 618 F.3d 1354, 1359 (Fed. Cir. 2010)). Wistron states that the term must still provide "context essential to understanding" the meaning of the term in the body of the claim. *Id.* (quoting *Seachange Int'l, Inc. v. C-Cor, Inc.*, 413 F.3d 1361, 1376 (Fed. Cir. 2005)). Wistron contends that the usage of "integrated circuit" in the body does not provide essential context to the invention.

Wistron acknowledges that claim 1 of "the '305 patent recites 'means to switch between the banks based on one or more external signals is provided on ***said*** integrated circuit,' " but argues that "this use can hardly be said to provide "essential context." Docket No. 104 at 6. According to Wistron, the "means to switch between banks" limitation was added to claim 1 from a dependent claim and, thus, cannot be said to be essential context since the term was not in claim 1 originally.

Docket *Id.* at 5–6. Wistron further notes that the "integrated circuit" is only found in the specification three times. *Id.* at 6.

Wistron also argues that limiting the claim to a single integrated circuit would exclude the preferred embodiment of Figure 2. Specifically, Wistron contends that the Figure 2 embodiment discloses multiple semiconductor chips, specifically gamma reference controller 210, gamma reference controller 220 and programming interface 230. Wistron asserts that Phenix's expert, Robert Murphy, agrees on this point. *Id.* at 6–7. According to Wistron, however, this position clashes with requiring claim 1 to be a single integrated circuit.

Wistron also argues that the embodiment of Figure 6 would also be excluded under Phenix's construction. Docket No. 104 at 7. Specifically, Wistron argues that the AG1818 embodiment of Figure 6 includes a programmable interface and elsewhere the specification teaches that the programmable interface may be a personal computer-based interface. '305 Patent at 7:13–14 ("PC based programming interface is available for prototyping and gamma optimization.").

<u>Analysis</u>

> In general, a preamble limits the invention if it recites essential structure or steps, or if it is "necessary to give life, meaning, and vitality" to the claim. Conversely, a preamble is not limiting where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.

Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc., 239 F.3d 801, 808 (Fed. Cir. 2001) (citations omitted).

Here, the term "integrated circuit" is not merely found in the preamble but also in the body of the claim. '305 Patent at Claim 1 ("means to switch between the banks based on one or more external signals is provided on said integrated circuit"). The means to switch "on said integrated

circuit" provides essential context to what is claimed, and the term "said" clearly references the preamble's disclosure of "an integrated circuit." *Id.* In this context, the "means to switch" is "on said integrated circuit," within which the other claimed elements are also found.

Further, the limitation that added "integrated circuit" to the body of the claim was added during prosecution by incorporating the subject matter of an allowable dependent claim (application claim 6) into claim 1. This highlights the importance of the limitation in the body of the claim. *See* Docket No. 100-3 at 67, 79, 99.

Wistron argues that this would exclude the embodiment of Figure 2 and that excluding embodiments is rarely correct. However, the body of claim itself makes the exclusion. As Wistron notes, the term "integrated circuit" is only utilized a few times in the specification; however, in one instance, it is utilized in relation to the single device embodiment of Figure 4B (as opposed to the separate devices of Figure 2):

> In one embodiment of the invention, the integrated circuit, termed the AG1818, is a programmable gamma reference generator with integrated output buffers to directly drive the source driver inputs of a display; in one embodiment the display is a TFT LCD. The circuit requires a single 3.3 volt supply, 1.5 mA operating current and consumes 10 uA in standby mode. FIGS. 4A and 4B show an alternative pin out of this embodiment.

'305 Patent at 5:30–37. In context of this passage and by noting the contrast between Figures 2 and 4B, it is clear that the '305 Patent discloses alternative embodiments, including single integrated circuits and multiple-devices configurations. Thus, the usage of "integrated circuit" in the claims provides further life and vitality to what is being claimed.

Wistron also argues that the '305 Patent provides that a programming interface that is PC-based may be utilized for prototyping. '305 Patent at 7:7–19. In light of the reference to a single integrated circuit provided in Figures 4A, 4B, 5 and 6 and the description that the programming interface of Figure 6 "allows the device to be programmed in-situ" ('305 Patent at 6:22–23), it is

clear that: (1) the PC-based programming interface is provided as an alternative embodiment and (2) the prototyping that provides an "alternate source" of Vpp does not alter the integrated circuit implementation of the figures and description of the '305 Patent. '305 Patent at 7:7–19, 5:30–7:6. In the briefing and during oral argument, Wistron further argued that it is not clear if "integrated circuit" is known to those in the art to refer to circuitry being formed on only one circuit, such as a single semiconductor chip. *See* Docket No. 123 at 37–38. However, such assertions conflict with the clear teaching of the specification, including the embodiments of Figures 4A, 4B, 5 and 6.

The extrinsic expert evidence, including that of Wistron's own expert, contradicts Wistron's argument as to what was generally well-known in the art at the time of the invention with respect to an integrated circuit being formed as a single device. *See* Docket No. 100-4 ¶¶ 31–33, 43; *see* Docket No. 100-8 at 89:23–90:11; *see also* Docket No. 100-17 ¶ 29. On balance, the Court finds Phenix's expert's interpretation of the meaning of "integrated circuit" to be correct and rejects Wistron's contention that an integrated circuit is not integrated on one semiconductor chip. *See Teva Pharm.*, 135 S. Ct. at 841.

In context of the claim itself and the specification, the preamble provides life, vitality and meaning to the claim, and thus, is properly included as a limitation of the claim.

The Court finds that the preamble of claim 1 is a limitation reciting one integrated circuit.

2. "non-volatile storage cells" (claims 1, 2, 4)

Phenix	Wistron	TI
Cells of a semiconductor memory that retain their stored data after power is removed and that restore the data when power is returned to the system, such as, for example, cells found in the following memories: analog floating gate non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM)	Memory cells storing analog voltages, which retain the stored voltages even when power is removed	analog non-volatile storage cells

The primary dispute is whether the term "storage cells" encompasses both analog and digital cells or if it is limited to analog cells.

<u>Positions of the Parties</u>

Phenix contends that one of ordinary skill in the art would understand that "non-volatile," in the context of semiconductor memories, would mean a type of memory cell that is capable of retaining a stored value even when power is removed. Docket No. 100 at 16. Phenix asserts that embodiments of the '305 Patent describe analog floating gate memory, which are types of memory cells that have an analog value. *Id.* However, according to Phenix, the claim term is not limited to analog and a person of ordinary skill in the art ("POSITA") would recognize that either analog or digital storage cells may be used. *Id.* Phenix contends its construction is consistent with known treatises. *Id.* at 18 n.62. Phenix notes that Wistron's expert, Richard Flasck, acknowledges that outside of the context of the '305 Patent, the term is understood to cover either digital or analog storage cells. *Id.* at 17.

Wistron contends that both the specification and claims demonstrate that "storage cells" is limited to analog. Wistron contends that storage cells are consistently referred to as "programmable analog floating gate memory cell" throughout the specification. Docket No. 104 at 10 (citing '305 Patent at 3:52, 4:11–20). Wistron points to the specification's statement that "[e]ach output is internally connected to an analog nonvolatile storage cell which can be written with 1,024 analog values, providing 10 bit resolution, or, said another way, to better than 15 mV resolution." *Id.* (quoting '305 Patent at 5:40–43). Wistron states that the prior art discussion teaches away from digital memory as being "quite expensive" and "unacceptable." Docket No. 104 at 10 (citing '305 Patent at 1:45, 2:9).

Wistron further argues that a digital storage cell would require the use of a digitial-to-analog converter ("DAC") and that the '305 Patent never discloses the use of a DAC. Rather, the '305 Patent compares the claimed invention to the resistor approach disclosed in the prior art, stating that a "[DAC] could perform this function in some ways better than the Select-On-Test resistors, but the cost is unacceptable." '305 Patent at 1:39–45. Wistron further argues that the '305 Patent's reference to the problems concerning the use of digital memory cells amounts to disclaimer. Docket No. 104 at 10–11 (citing '305 Patent at 2:4–12). Wistron also contends that the inventor's testimony supports finding that the '305 Patent was directed to an analog approach. *Id.* According to Wistron, this further supports the conclusion that the digital approaches in general were disclaimed. *Id.* at 11.

Wistron next points to independent claim 6, which states that the programming of the cells is done by analog methods. '305 Patent at claim 6, 8:18–19 ("applying incremental voltage pulses"). Wistron notes that dependent claim 4 provides that "said non-volatile storage cells hold

analog voltage values which are a constant fraction of said gamma reference voltage signals." '305 Patent at claim 4.

Wistron argues that Phenix is broadening the claims beyond the narrower disclosure of the specification and that such broadening is improper when the patent "repeatedly and consistently characterizes" a claim term in a particular manner. Docket No. 104 at 12-16 (citing *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296 (Fed. Cir. 2011); *UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816 (Fed. Cir. 2016); and *Profoot, Inc. v. Merck & Co.*, 663 F. App'x 928, 932 (Fed. Cir. 2016)). Wistron lists sixteen references in the specification in which "analog" inputs, outputs or memory cells are recited. Docket No. 104 at 14–15.

Wistron notes that Phenix's proposed construction includes a list of memories and argues that the list should not be incorporated into the Court's construction because only one of the listed memories ("analog floating gate non-volatile memory") is disclosed in the intrinsic record. Docket No. 104 at 17–18.

TI notes that the parties and experts agree that, outside the context of the '305 Patent, a non-volatile storage cell may store either digital values or analog values. Docket No. 104 at 17 (citing Docket No. 104-9 (Baker Decl. – TI expert) ¶ 44; Docket No. 104-3 (Flasck Decl. – Wistron Expert) ¶ 40; Docket No. 104-10 (Murphy Decl. (Oct. 7, 2018) – Phenix Expert) ¶ 36; Docket No. 104-7 (Murphy Decl. (July 16, 2018)) ¶ 36). TI asserts that the only dispute is whether, in the context of the '305 Patent, the patentee disavowed non-volatile storage cells that store digital values. Docket No. 104 at 17. TI contends its proposal should be adopted for two reasons: first, the specification consistently discloses analog cells and second, the patent disparaged digital storage. *Id.*

As to Phenix's argument regarding storage of digital voltages as compared to digital values, TI contends that non-volatile storage refers to cells that store a voltage to represent a value, and a digital non-volatile storage cell stores a voltage within a broad, imprecise range that represents a digital value (e.g., "1" or "0"). TI states that an analog non-volatile storage cell stores a precise voltage that represents the actual output voltage, which may be one of potentially many (e.g., more than 1,000) voltage levels. Docket No. 104 at 16–17.

TI contends that when using digital storage cells to output analog values, a DAC must be used; however, a DAC is not required when outputting analog values from analog storage cells. *Id.* at 18. TI then points to all the usages of "analog" in the specification, further noting that the patent disparages the use of DACs by stating that "the cost is unacceptable." Docket No. 104 at 18–19 (quoting '305 Patent at 1:41–45). TI notes that, in the patent, drivers 340–347 are directly connected to analog floating gate memory cells 330–337 to output the analog values without the use of a DAC ('305 Patent at 4:4–21, Figures 3, 6) and that Phenix's prior expert, William Owen, agreed in the *IML* litigation that the '305 Patent is directed toward analog technology. Docket No. 104 at 19.

Phenix argues that Defendants conflate "storage cells" with "memory." Phenix asserts that semiconductor memories that provide digital and analog values are typically composed of the same non-volatile storage cells. *Id.* at 17. Phenix asserts that storage cells are building blocks that simply hold charge, that are used to implement memory and that they are agnostic as to whether the memory outputs analog or digital values. Phenix states that the cells simply hold charge and that what the charge represents and how it is interpreted (i.e., analog or digital) is up to the memory architect. *Id.* at 18–19.

In response to Defendants' assertion that digital memories require the use of digital-to-analog converters ("DAC"), Phenix points to Mr. Murphy's testimony that a digital memory does not utilize a DAC. Docket No. 100 at 19–20. Phenix contends that to the extent DACs are used with digital memory, the DAC is part of the driver circuit that drives the LCD panel, not the storage cell. *Id.* at 19. Phenix further asserts that the '305 Patent does not teach away from the use of digital representations because the embodiments of the '305 Patent are mixed-signal designs that have elements of both analog and digital implementations all on the same integrated circuit. Docket No. 100 at 20. Phenix notes that the prior art section discloses an analog solution using a resistor tree. Docket No. 100 at 20 (citing '305 Patent at 1:39–2:3). Phenix notes that the patent describes "more recent" approaches in two patents that eliminate the resistors but teach "complex digital approaches to this 'analog' problem[.]" '305 Patent at 2:4–9. Phenix argues that this does not teach away from using all digital approaches, but merely notes that the two prior art patents disclose complex expensive circuitry embodiments. Docket No. 100 at 20. *Id.* at 20-21.

Phenix points to Wistron's PTAB expert's declaration in support of its argument that the '305 Patent is not limited to analog technology:

> A POSITA would understand the term 'non-volatile storage cells' to ***apply to the storage of both analog and digital values in the storage cells*** because the term 'non-volatile' storage cells can be used to describe any of analog floating gate non-volatile memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash EEPROM, Ultraviolet EPROM (UVEPROM), and Non-Volatile Random Access Memory (NOVRAM).

Docket No. 100 at 21, ¶ 45(emphasis added). Phenix also notes that Wistron's PTAB construction was nearly identical to Phenix's current construction. *Id.* at 21–22.

Lastly, Phenix contends that the doctrine of claim differentiation teaches that claim 1 is not limited to analog techniques in light of dependent claim 4, which adds the term "analog." Docket No. 106 at 3.

Analysis

The parties and experts substantively agree that in an ordinary meaning a "non-volatile storage cell" may store either digital values or analog values. The Defendants primarily argue two points for limiting the term: (1) every embodiment of the '305 Patent expressly recites analog storage, and (2) the '305 Patent criticizes digital storage approaches due to their cost and complexity while repeatedly extolling the virtues of an analog approach. Docket No. 104 at 14, 17.

As to the first argument, the specification does recite "programmable analog floating gate memory cells" and "analog storage cells" as having "analog inputs" or "analog voltage values." *Id.* at 3:48–4:21, 5:38–49. There also does not appear to be a dispute that the only embodiment of the specification is an analog non-volatile storage cell. However, "it is improper to read limitations from a preferred embodiment described in the specification – even if it is the only embodiment – into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co.*, 358 F.3d at 913. Within the description of the embodiment in the specification, Defendants have not shown a clear intention to limit the ordinary meaning of the term. The primary focus of the description of the storage cells is the programmable nature of the storage cells, not a distinction between analog and digital storage cells. *See* '305 Patent at 3:6–7:19.

The specification repeatedly refers to "analog floating gate memory cells," "analog storage cell," and "analog nonvolatile storage cell." *Id.* at 3:48–4:21, 5:38–49. The modifier "analog" indicates that "storage cells" themselves are not inherently analog. *See Phillips*, 415 F.3d at 1314 ("[T]he claim term in this case refers to 'steel baffles,' which strongly implies that the term 'baffles' does not inherently mean objects made of steel."). The language of other claims also

indicates that the "storage cells" themselves are not inherently analog. '305 Patent at claims 4, 13 ("wherein said non-volatile storage cells hold analog voltage values…"); *see also Phillips*, 415 F.3d at 1314–15 ("Other claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term.").

Despite this, Defendants allege that two sentences of the specification sufficiently disparage digital approaches to support limiting the claimed invention to analog technology. '305 Patent at 1:41–45 and 2:7–8. These two sentences do not meet the Federal Circuit standards of being "clear and unmistakable," "exacting" and "repeated derogatory statements." *Openwave Systems, Inc. v. Apple Inc.*, 808 F.3d 509, 513–14 (Fed. Cir. 2015); *GE Lighting Solutions*, 750 F.3d at 1309; *Cordis Corp. v. Boston Sci. Corp.*, 561 F.3d at 1329. Further, they do not show that "the specification goes well beyond expressing the patentee's preference[,]" and they are not more than "mere criticism[s] of a particular embodiment encompassed in the plain meaning of a claim term." Moreover, these sentences could be "amenable to multiple reasonable interpretations." *Openwave Systems*, 808 F.3d 513–14; *Thorner*, 669 F.3d at 1366–67.

The alleged disparagement is not a general disparagement of digital circuits because the prior art that is criticized includes both analog and digital approaches. '305 Patent at 1:28–37, 1:46–2:4, 2:6–9, Figure 1. Rather, the question presented is whether digital storage cells have been disparaged as compared to analog storage cells. Nowhere in the specification is there any contrasting between analog and digital storage cells. The storage cell's ability to be programmed and changed appears to be the primary advantage distinguishable over the prior art resistor approaches discussed in the '305 Patent. '305 Patent at 1:28–37, Figure 1. Additionally, the Summary of the Invention clearly describes the invention in the context of the importance of programmability. '305 Patent 2:15–38.

There is no dispute that the allegedly disparaging sentences do not explicitly mention digital versus analog memory cells. The '305 Patent references the resistor approach, which involves manual set-up that cannot be changed thereafter. '305 Patent at 1:39–45. The patent then states that other approaches, such as the use of a DAC, could replace resistors, but the cost is unacceptable. '305 Patent at 1:41–45 ("Digital to Analog Converters (DACs) all could perform this function in some ways better than the Select-On-Test resistors, but the cost is unacceptable."). This statement does not clearly indicate that replacing the resistors with programmable storage cells that store digital values is unacceptable or that the invention does not include digital storage cells. Instead, it merely criticizes approaches that use DACs in place of the resistors because they are expensive.

Defendants point to the specification for further support, noting that it states "quite complex approaches" are used to replace the resistors, specifically "quite complex digital approaches." '305 Patent at 2:4–9. This statement, however, is not tied to the type of memory that is utilized and, thus, fails to meet the high bar of disavowal. The specification does not state that digital approaches are complex or undesirable because they use digital storage cells, nor does it define what constitutes "acceptable" cost. The next sentence after the alleged disparagement merely states that it would be "desirable" to design a gamma reference architecture that "provides reprogrammable capability and achieves acceptable cost." *Id.* at 2:10–12.

Ultimately, the passages relied upon by Defendants fail to satisfy the high bar of disparagement or disavowal.

The Court construes "non-volatile storage cell" to mean "memory cells which retain stored data even when power is removed."

3. "circuits for programming" (claims 1, 5)

Phenix	Wistron	TI
Plain and ordinary meaning -------------------------------- Alternatively, the term is written as means-plus-function subject to § 112 ¶ 6 **Function**: programming non-volatile storage cells **Structure**: FIG. 3 (Programming Engine 310); TABLE 1 (R/W, VIN (Analog Input)); FIG. 6 (Programming Interface, Vpp), FIG. 4A (Vpp), FIG. 4B (pin 2), FIG. 5 (Vpp); the '305 patent as to the above at Abstract, 3:17–29 (FIG. 2), 4:22–32, 6:22–53	Indefinite	This term is written as a means-plus-function subject to § 112 ¶ 6 **Function**: programming **Structure**: '305 Patent, 6:22–67; Fig. 4A (Vpp, Aout, A0–A1, B0–B2); Fig. 4B (Vpp, Aout, A0–A1, B0–B2); Fig. 5 (Vpp); Fig. 6 (Programming Interface, Vpp, Aout, A0–A1, B0–B2)

The term in question is found in the following claim 1 limitation: "circuits for programming coupled to a multiplexer for addressing and programming said storage cells." Phenix contends that the term is not a means-plus-function element. Wistron contends that the specification does not disclose the programming circuitry in sufficient detail to provide corresponding structure. If it is a means-plus-function term, Phenix and TI dispute what should and should not be included in the structure.

Positions of the Parties

According to Phenix, the specification teaches two different types of circuits for programming: (1) a circuit for programming using a high voltage that is generated internally and (2) circuits that use high voltage pulses that are brought in externally via a pin on an integrated circuit. Docket No. 100 at 23–24. Phenix contends that the first type is shown in Figure 2 using

a high-level architectural diagram where programming interface circuitry is illustrated as a functional block named "Programming Interface 230." According to Phenix, the specification discloses circuits for programming using a "Tracking Mode" where the writing and programming is accomplished using an Analog Input (AIN), the address inputs (A2–A0) and a read/write (R/W) control pin. Phenix asserts that more detail is provided in Figure 3, where the programming of the non-volatile storage cells is shown in reference to a functional block "Programming Engine 310." Phenix states that Programming Engine 310 uses as inputs an Analog Input and a read/write (R/W) control pin to program a gamma reference controller 300. Phenix contends that the descriptions of various pin parameters for this embodiment are shown in Table 1. Docket No. 100 at 24. Phenix further points to the specification as describing this operation:

> During normal operation, the R/W pin is pulled High and the reference voltage outputs will reflect the value last programmed into the nonvolatile memory cells.
>
> The writing or programming operation is accomplished by first selecting the output or channel of the device to be programmed with the A2–A0 inputs. At this point, R/W on the device to be written is driven low and the device enters Tracking Mode. During Tracking Mode, the output of the selected channel tracks the input voltage on the Analog Input. (An optional internal voltage multiplier converts the 0–3V Analog Input to a 0–10 Volt output.)
>
> Once the desired voltage is found by varying the Analog Input for a particular channel, the R/W signal is driven high and the value on the Analog Input is written into the nonvolatile memory for the output channel selected by the A2-A0 inputs.

'305 Patent at 3:14–29. As to how the circuitry operates in programming, Phenix lists the programming steps and structures for the embodiment of Figures 2 and 3:

TABLE A – Programming Steps for FIGS. 2 and 3					
Order	Action	Structure/Pins	Pin Values	Patent Cite	Comment
Step 1	Select the cell to be written	A0, A1, A2	Binary cell address selection	3:17-19 and Table 1	Location of memory cell to be written determined.
Step 2	Enter Tracking Mode	R/W	Pin driven LOW for track mode operation	3:19-21, 4:22-27 and Table 1	The device enters a "Tracking Mode" for writing to a cell where the channel outputs follow or "track" the Analog Input. The voltage value on the Analog Input is written to a memory cell.
Step 3	Select the voltage to be written to the cell	V_{IN} (Analog Input)	Voltage applied to Analog Input	3:22-23; 25-29 and Table 1	The voltage on the Analog Input is varied until the desired voltage is reached. Output channels (CH0 – CH7) track the Analog Input.
Step 4	Write Cycle	Programming Engine 310, R/W, V_{IN} (Analog Input)	R/W rising edge to HIGH; Analog Input stored	3:25-29, 4:26-31 and Table 1	Memory cell written with voltage value on the Analog Input.

Docket No. 106 at 5.

Phenix contends that the second type of circuit is shown by the Programming Interface of Figure 6 which uses externally generated high voltage pulses provided on the Vpp pin. Phenix contends that dependent claim 5 relates to this embodiment because the claim states that "circuits for programming require an external source for the high voltage programming means." Docket No. 100 at 25–26. As to the steps and structure for the embodiment of Figure 6, Phenix points to the programming steps:

TABLE B – Programming Steps for FIG. 6					
Order	Action	Structure/Pins	Pin Values	Patent Cite	Comment
Step 1	Select program mode	A0, A1, B0, B1, B2, VPP	1, 1, 1, 1, 1 and VPP is set to HIGH	6:37-40, FIG. 4A and FIG. 4B	Since there is no R/W pin, the device uses these pins to enter a programming state.
Step 2	Select bank address	B0, B1, B2, VPP	VPP pulsed. Binary bank address selection; VPP pulsed again.	6:41-42	Bank to be programmed is selected when VPP pulsed. VPP pulsed again to latch the bank.
Step 3	Select the memory cell	A0, A1, A2, B0, B2	Binary memory cell address selection	6:42-44	Memory cell selected using binary data on 5 pins.
Step 4	Write Cycle	Programming Interface, VPP	VPP pulsed. Programming of memory cell initiated by pulsing VPP with adjustable pulses between 8-14 volts.	6:44-47	VPP pulsed a third time to select memory cell address and begin write cycle. Memory cell written with voltage value.
Step 5	Return to Read mode	A0, A1, B0, B1, B2, VPP	1, 1, 1, 1 and VPP pulsed.	6:47-50	VPP pulsed again to return to read mode.

Docket No. 106 at 6.

Phenix quotes *Williamson* for the proposition that the term is not a means-plus-function term where "the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure" and that the term is only a means term if "the claim term fails to recite sufficiently definite structure or else recites function without reciting sufficient structure for preforming that function." *Williamson*, 792 F.3d at 1348. Phenix asserts that the term does not include the word "means" and that the claim recites sufficiently defined structure to a POSITA such that the term is not a means-plus-function term under *Williamson*. Docket No. 100 at 26. According to Phenix, a POSITA would understand that, for non-volatile memory, high voltages and circuits to carry high voltages are required to program the cells. Docket No. 100 at 26. Further, Phenix argues that in light of the specialized nature of the circuits for programming needed for erasing and writing non-volatile storage cells, a POSITA would not

understand this term as reciting generic circuits for programming. *Id.* at 26–27. Phenix cites Mr. Murphy's testimony for the position that the knowledge on circuits for programming and the Programming Engine ('305 Patent at Figure 3, block 310) was in the prior art decades before the '305 Patent was filed. *Id.* at 29. Phenix contends that the claims and specification make clear that "circuits for programming" refers to programming "non-volatile storage cells." *Id.* Thus, Phenix argues, a POSITA would know the "circuits" are limited to a narrow scope of circuits as such programming was well-known to be a specific high voltage programming. Docket No. 106 at 8.

Wistron contends that the only disclosure of any structural components in the '305 Patent for this term is the "programming engine or interface 310," which "comprises an Analog Input which will be used to set the reference voltage level and a R/W control signal for a corresponding gamma reference controller." Docket No. 104 at 20 (quoting '305 Patent at 3:48–4:8). Wistron cites to testimony from its expert, Mr. Flasck, and Phenix's expert, Mr. Murphy, for the proposition that the circuitry for high voltage programming is specialized. *Id.* at 20–21. Wistron contends that given the specialized nature of the circuits in question, providing a single input and a control signal falls short of the disclosure required to delineate the scope of the claim. *Id.* Wistron contends that the patent merely recites functionality without the structure to perform the functionality. Without any way of knowing what the circuits for programming consist of or how they are constructed, it is impossible to determine the scope of the claims. *Id.* at 21–22.

TI contends that under *Williamson*, the term is a means-plus-function term even though "means" is not recited. TI relies on its expert's assertion that "circuits" does not provide definite structure. Docket No. 104 at 22. Further, TI contends that even Phenix's expert stated that "circuits" is very broad and does not give specific indication of a particular design. *Id.* at 22–23. TI acknowledges that the Federal Circuit has found that use of "interface" together with "circuit"

provides sufficient structure to avoid means-plus-function claiming. *Id.* (citing *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1374 (Fed. Cir. 2003)). However, TI asserts that *Apex* does not stand for the proposition that "circuits" always connotes structure. Rather, TI contends that all the experts in this matter have acknowledged that "circuits for programming" is a very broad term that does not identify specific programming circuits. *See* Docket No. 104 at 23–24.

Analysis

The term in question ("circuits") is not a nonce word in the context of the claim language, which discloses "circuits for programming" of non-volatile storage cells. The Federal Circuit has repeatedly and consistently found that, in the electronic arts, "circuit" or "circuitry" terms connote sufficient structure to avoid means-plus-function claiming. The rationale of those cases applies equally here. In *Apex*, the Federal Circuit noted that:

> The threshold issue for all the limitations involving the term "circuit" is whether the term itself connotes sufficient structure to one of ordinary skill in the art to perform the functions identified by each limitation. The district court determined this term, by itself, did not connote sufficient structure and prematurely ended its analysis at this threshold issue. While we do not find it necessary to hold that the term "circuit" by itself always connotes sufficient structure, the term "circuit" with an appropriate identifier such as "interface," "programming" and "logic," certainly identifies some structural meaning to one of ordinary skill in the art.
>
> The term "circuit" is defined as "the combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function." *Dictionary of Computing*, 75 (4th ed.1996).
>
> In light of this definition, it is clear that the term "circuit," by itself connotes some structure. In the absence of any more compelling evidence of the understanding of one of ordinary skill in the art, the presumption that § 112 ¶ 6 does not apply is determinative.

Apex, 325 F.3d at 1373.

Here, "circuits" is accompanied by an "appropriate identifier such as 'interface,' 'programming' and 'logic[.]' " *Id.* The term itself explicitly references "programming." Further,

the claim and the totality of the specification make clear that these circuits are directed to programming non-volatile storage cells.

Defendants contend that the claim term is overly broad; however, the critical inquiry is whether the words of the claim are understood by a POSITA to have a sufficiently definite structure. Wistron's expert, Mr. Flasck, acknowledges that "programming" circuits connotes "specialized electrical circuits" to those skilled in the art. Docket No. 104-3 ¶ 56. The Federal Circuit has addressed this issue:

> We have previously held on several occasions that the term "circuit" connotes structure. *See MIT v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006) ("[D]ictionary definitions establish that the term 'circuitry,' by itself, connotes structure."); *see also Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320-21 (Fed. Cir. 2004) (holding that the term circuit is not a means-plus-function limitation when the patent provides "a recitation of the respective circuit's operation in sufficient detail to suggest structure to persons of ordinary skill in the art"); *Apex*, 325 F.3d at 1373 ("[T]he term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art."). In *Abacus*, we said,
>
>> The claim language here too does not merely describe a circuit; it adds further structure by describing the operation of the circuit. The circuit's input is "appearance signals" produced by the scanner; its objective is to "interactively introduce[e] [sic] aesthetically desired alterations into said appearance signals"; and its output is "modified appearance signals." This description of the operation of the circuit is sufficient to avoid 112 ¶ 6.
>
> 462 F.3d at 1356 (citation omitted).
>
> *Abacus* establishes that in determining whether the word "circuit" invokes means-plus-function claiming, the pivotal issue is "whether the [circuit limitation] as properly construed recites sufficiently definite structure." *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n,* 161 F.3d 696, 704 (Fed.Cir.1998) (emphasis added). A description of the circuit's operation may provide sufficiently definite structure, *Abacus*, 462 F.3d at 1356, as can certain "adjectival qualifications," *Apex*, 325 F.3d at 1374 ("interface circuit"). Nevertheless, not just any adjectival qualification or functional language will suffice. *See Abacus*, 462 F.3d at 1362–63 (Michel, C.J., dissenting). The proper inquiry is whether the claim limitation itself, when read in light of the specification, connotes to the ordinarily skilled artisan sufficiently definite structure for performing the identified functions. *Apex*, 325 F.3d at 1373.

Power Integrations, Inc. v. Fairchild Semiconductor Intern., Inc., 711 F.3d 1348, 1364–65 (Fed. Cir. 2013).

In *Power Integrations*, the Federal Circuit noted that the term in question ("soft start circuit") could "be achieved in a variety of ways" and may cover "a broad class of structures." *Id.* at 1365. The Court concluded:

> Nevertheless, viewed in the context of the claimed invention, the function recited is sufficiently clear, and definitely described, to suggest to the ordinarily skilled artisan a defined class of structures. As in *Abacus*, we have an input to the circuit (the oscillation and frequency variation signals), a straightforward function (comparing of the magnitudes of these signals), and an output (the signal provided to the drive circuit based on the comparison). This is sufficient structure in the context of the claimed invention to avoid the ambit of means-plus-function claiming.

Id. Here, the circuitry is clearly defined in the claim and specification as programming circuitry. Further, the claim provides additional structural limitations because it recites the coupling of the circuits. '305 Patent at claim 1 ("circuits for programming coupled to a multiplexer.").

Recently, when construing the term "unit," the Federal Circuit contrasted the nonce word "unit" with "circuits:"

> In *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364 (Fed. Cir. 2003), we considered whether claim limitations reciting "circuits" were subject to § 112 ¶ 6. We began by noting that the term "circuit," which one dictionary defines as "the combination of a number of electrical devices and conductors that, when interconnected to form a conducting path, fulfill some desired function," "by itself connotes some structure," and explained that "the term 'circuit' with an appropriate identifier such as 'interface,' 'programming' and 'logic,' certainly identifies some structural meaning to one of ordinary skill in the art." *Id.* at 1373. We then observed that nothing in the specification or prosecution history was inconsistent with the ordinary meaning of the term "circuit," and pointed out that the Raritan's experts' testimony "show[ed] only that the term 'circuit' is understood by one of ordinary skill in the art as a very broad term and that one of the accused products included several of the circuit elements." *Id.* at 1373–74.

Diebold Nixdorf, Inc. v. International Trade Commission, 899 F.3d 1291, 1301 (Fed. Cir. 2018).

Against this background, the Court finds that "circuits for programming" connotes sufficient structure and is not a means-plus-function term.

The Court finds that the term "circuits for programming" has its plain and ordinary meaning.

4. "programming said storage cells" (claim 1)

Phenix	Defendants
Plain and ordinary meaning or "writing to a storage cell by depositing or removing charge"	writing an analog reference voltage to the storage cells

The parties dispute whether the term is limited to writing analog voltages.

Phenix contends that techniques for programming storage cells were known for over three decades prior to the '305 Patent. Docket No. 100 at 31. Phenix asserts that a POSITA would recognize that the techniques described in the patent were just embodiments of high voltage programming of non-volatile storage cells. *Id.* Phenix further asserts that a POSITA would understand that the act of programming refers to adding or removing charge from a non-volatile storage cell with no restriction on whether that charge represents an analog or digital value. *Id.*

Defendants acknowledge that "outside the context of the '305 patent, programming a storage cell may involve either writing an analog reference voltage or a digital value." Docket No. 104 at 26. However, Defendants assert that the patentee disavowed digital non-volatile storage for the same reasons as discussed above with respect to the "non-volatile storage cell" term. *Id.* Defendants cite to six passages of the specification which describe the programming in relation to analog inputs or analog memory cells. *Id.* at 26–27.

Analysis

The issue presented by the parties is the same analog-versus-digital dispute addressed above with respect to the "non-volatile storage cell" term. *See supra* at 18–26. For the same reasons discussed above, the Court rejects Defendants' argument that the patentee disavowed digital non-volatile storage.

The Court construes "programming said storage cells" to mean "writing data to a storage cell.

5. "drivers" (claim 1)

Phenix	Wistron	TI
One or more circuit elements that change one or more characteristics of an electrical signal and used to control another circuit or component	Analog sub-circuit that provides isolation between a signal generating element and a signal receiving element to preserve signal integrity	TI takes no position on this term and does not join this section

The term is found in the following phrase: "drivers connected to said storage cells and to the plurality of outputs." The parties dispute whether "drivers" limits the claimed invention to an analog invention and whether Phenix's construction is overbroad.

Positions of the Parties

Phenix identifies the drivers in Figure 3 as elements 340, 341, *et. seq.*, which are connected to storage cells 330, 331, *et. seq.*, and connected to the outputs shown as CH0, CH1, *et. seq.* Phenix also points to the passage of the specification that states that the integrated circuit (such as shown in Figure 4B) has "integrated output buffers to directly drive the source driver inputs of a display; in one embodiment the display is TFT LCD." Docket No. 100 at 33–34.

Phenix contends that there is no clear disclaimer or lexicography limiting the drivers to the role of isolating parts of a circuit. *Id.* Phenix contends that one of ordinary skill in the art understands that the triangle symbols labeled as 340, 341, 346 and 347 represent linear amplifiers

that are commonly used in analog circuits. Phenix contends that though a linear amplifier may provide some isolation, a linear amplifier, by its plain terms, is inserted into a circuit for the purpose of amplifying a signal in a linear fashion. *Id.* at 35. Phenix also points to its expert testimony for the position that "drivers" is not limited to the linear amplifiers. *Id.* Phenix states that even Wistron's expert, Mr. Flasck, agrees that the industry term "source driver" is a component of LCD panels and includes DACs. *Id.*

Wistron contends that the primary issue is whether the invention is an analog invention. Wistron states that its expert, Mr. Flasck, has testified that "[i]n the field of electronics, a driver is a sub-circuit that provides isolation between a signal generating element and a signal receiving element." Docket No. 104 at 33. Wistron further states that "the term 'driver' is synonymous with 'buffer' and often is a unity gain amplifier." *Id.*

Wistron objects to Phenix's construction as being drafted in a manner that encompasses DACs. Wistron notes that the patent disparaged the use of DACs by stating the "cost is unacceptable." Docket No. 104 at 34 (quoting '305 Patent at 1:41–45). Wistron contends that the patent taught that prior art digital approaches were undesirable, including U.S. Patent No. 6,593,934 (Liaw). Wistron points to Liaw as indicating that DACs and drivers are different structures as indicated by DAC 32 and driver 34 of Liaw:

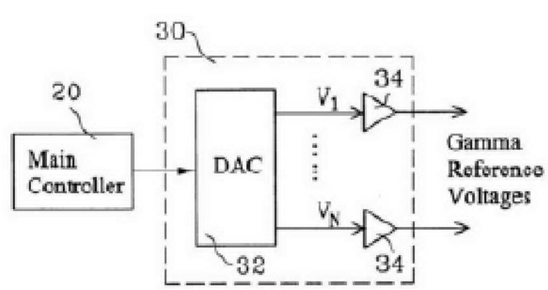

FIG. 11

Docket No. 104-8 (Liaw) at Figure 11.

As to the use of "source drivers," Wistron contends those are specialized circuits that provide the analog voltages to an LCD panel. Docket No. 104 at 35. Wistron contends that its expert, Mr. Flasck, and Phenix's expert, Mr. Murphy, acknowledge that "source drivers" and "drivers" are different. Wistron contends that whether "source drivers" have DACs is irrelevant. *Id.*

Analysis

The "analog" issue has been addressed above. *See supra* at 18–26. Wistron has not provided argument that ties the "analog" issue sufficiently to the term "driver" to warrant consideration of limiting the term "driver" beyond its ordinary meaning. Wistron asserts that the term "isolation" should be included in the Court's construction but fails to cite to any intrinsic evidence in support; rather, Wistron relies solely on expert testimony. Wistron does not address common drivers such as buffers and amplifiers that might not have isolation functions. Wistron does acknowledge, however, that "the term 'driver' is synonymous with 'buffer' and often is a unity gain amplifier." Docket No. 104 at 33; *see also* Docket No. 104-3 ¶¶ 65–67 (noting that the drivers in Figure 6 utilize the standard electrical symbol for a buffer). Wistron notes that such buffers and amplifiers are the kinds of structures that would perform the function that Wistron proposed in its construction. Docket No. 123 at 101.

On the other hand, Phenix's construction is so broad that it could be interpreted to encompass practically every electrical circuit. At the hearing, Phenix agreed to a construction of "buffer or amplifier."

The Court construes "drivers" to mean "buffers or amplifiers."

6. "predetermined gamma reference voltage signal display condition" (claim 1)

Phenix	Wistron	TI
A display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user	Indefinite	Agrees with Phenix

The parties dispute whether the term has meaning and, specifically, the parties dispute the meaning of "display condition."

<u>Positions of the Parties</u>

Phenix contends that a POSITA would understand how to select the necessary gamma correction reference voltages for the desired display condition that needed correction and cites to the following language of the specification in support: "the invention is a programmable buffer integrated circuit which can be programmed to output a set of gamma correction reference voltages to be used in Liquid Crystal Displays (LCDs)." '305 Patent at 2:16–19.

Phenix notes that the '305 Patent's Abstract provides that "[m]ultiple sets of values can be programmed to provide different gamma correction curves for different user or application requirements." According to Phenix, the '305 Patent explains this further:

> In one embodiment the AG 1818 has capacity to store and retrieve eight independent banks or groups of reference voltages. The banks of gamma voltages are stored and selected through the three address inputs BO, Bl, B2. This allows the gamma voltages to be changed either for dynamic gamma correction or application based gamma variation. This feature can also be used to switch between different gamma settings based on the information to be displayed for implementing dynamic gamma correction. A block diagram in FIG. 6 illustrates one alternative embodiment.

Id. at 5:50–59.

Phenix states that the ’305 Patent teaches that the integrated circuit “has capacity to store and retrieve eight independent banks or groups of reference voltages. . . . This allows the gamma voltages to be changed either for dynamic gamma correction or application based gamma variation.” *Id.* at 5:50–55. According to Phenix, the ’305 Patent teaches a programmable device where a POSITA loads into its memory banks the desired gamma reference voltages. *Id.* at 6:68–7:3 (“As mentioned previously, this programming step can take place prior to mating the gamma reference chip with a display wherein a predetermined set of voltage values is stored.”). Phenix asserts that this feature can also be used to switch between different gamma settings based on the information to be displayed for implementing dynamic gamma correction and that the patent contains several examples of the circumstances motivating, changing or correcting the display condition, including temperature, brightness, applications and user preference. Docket No. 100 at 37 n.137 (citing ’305 Patent at 7:20–32). Phenix contends that Wistron’s expert, Mr. Flasck, understood the meaning of “display mode” even though he did not understand “display condition.” *Id.* (citing Docket No. 100-8 at 166:11–167:15). Phenix also notes that TI’s expert, Dr. Jacob Baker, testified that a POSITA would understand the meaning of this term. *Id.* Finally, Phenix notes that during PTAB proceedings, Wistron and its experts cited references for disclosing “a predetermined gamma reference voltage signal display condition” without uncertainty as to the term meaning. *Id.* at 38.

Wistron contends that Phenix and TI’s construction and the claim term itself uses the term “display condition,” which does not appear anywhere in the specification of the ’305 Patent. Wistron contends that the ’305 Patent discloses storing a “predetermined set of voltage values” in storage cells, testing the display so as to achieve a “predetermined light matching for a display” and saving gamma reference voltage values for the same, and matching the output of a sensor to a

"predetermined application condition." Docket No. 104 at 35 (citing '305 Patent at 6:67–7:3, 7:23–27, 7:30–33). Wistron contends that none of these passages actually explain what a predetermined gamma reference voltage signal display condition is.

Wistron acknowledges that "application condition" is described in the specification. Docket No. 123 at 105. However, Wistron contends that Phenix is wrong in stating that the phrase "application condition" in the specification means the same thing as claim 1's "display condition." Docket No. 104 at 36. According to Wistron, the surrounding claim language makes clear that a "display condition" is some form of the gamma correction voltages stored in memory. '305 Patent at claim 1 ("said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition."). Wistron also contends that the '305 Patent discloses that a "predetermined application condition" is used to "select[] the corresponding gamma value set" for storage. '305 Patent at 7:30–32. Wistron argues that if the "application condition" is selecting the set of gamma reference voltage values stored in memory, it cannot be the same as the stored gamma value set. Wistron contends that Phenix's proposed construction merely rearranges the words of the term and adds examples of factors which might influence a "display condition" but still fails to explain what a "display condition" actually is." Docket No. 104 at 37.

Analysis

The Court finds that the arguments and interpretation of the specification provided by Phenix are correct. Though "display condition" does not appear in the specification, the specification, as a whole, provides sufficient meaning such that the term is not indefinite. Specifically, the specification provides that a set of voltages provided in a given bank gives the desired outcome on the display based on the application, environmental factors, user preference,

manufacturing adjustments, etc. The "display condition" is set based on the application conditions, environmental factors, user preferences and manufacturing adjustments. '305 Patent at 2:16–28, 5:50–59, 6:68–7:3, 7:20–32 (describing "application conditions"). Further, claim 1 states "wherein said non-volatile storage cells are organized into two or more banks of cells wherein each bank contains a predetermined gamma reference voltage signal display condition." This is consistent with the specification's disclosure of dynamic and application specific gamma correction and that the bank based voltages "can also be used to switch between different gamma settings." '305 Patent at 5:50–59. In the context of the intrinsic record, the Court finds that the term is sufficiently definite to provide meaning.

The Court finds that "predetermined gamma reference voltage signal display condition" means "a display condition established by the predetermined gamma reference voltage signals based on the application that is being displayed, external environment such as temperature and ambient light, or the personal preference of the user."

7. "means to switch between the banks based on one or more external signals" (claim 1)

Phenix	Wistron	TI
The term is written as means-plus-function subject to § 112 ¶ 6 **<u>Function</u>**: Switching between the banks based on one or more external signals **<u>Structure</u>**: the '305 patent at 5:50–59; FIG. 4A, Pin Descriptions (B0–B2); FIG. 4B Pinout (pins 20, 22, 23); FIG. 6 (B0, B1, B2, Bank Select)	Indefinite	This term is written as a means-plus-function subject to § 112 ¶ 6 **<u>Function</u>**: switching between the banks based on one or more external signals **<u>Structure</u>**: '305 Patent, 5:50–6:21; 6:34–53; Fig. 4A (B0–B2); Fig. 4B (pins 20, 22, 23); Fig. 5 (Tdamp); Fig. 6 (Bank Select, B0, B1, B2)

Wistron contends that the '305 Patent does not disclose any circuitry that actually performs the switching function. TI generally agrees with Phenix but contends that the damping circuitry must be included in the corresponding structure and that the use of the pins for programming must also be referenced in the corresponding structure.

Positions of the Parties

Phenix contends that a POSITA would understand that the one or more bank select input pins on an integrated circuit is the structure disclosed in the '305 Patent. Docket No. 100 at 39. Phenix contends that this corresponds to pins B0–B2 of Figure 4A, Pins 20, 22 and 23 of Figure 4B, and inputs B0, B1, and B2 of Figure 6. *Id.* at 39–40. Phenix contends that the functional block identified as "Bank Select" in Figure 6 would be understood by a POSITA as having the circuitry known in the prior art for selection a bank. *Id.* at 40.

Phenix objects to TI's construction's importation of the internal damping circuitry. *Id.* Phenix contends that this circuitry is used to "prevent display artifacts" and is not part of the switching function. *Id.* at 40. According to Phenix, this structure relates to an embodiment in which the bank select pins are also utilized to program various states of the integrated circuit, rather than the claimed switching function. *Id.*

Wistron contends that the '305 Patent does not disclose structure that actually performs the switching function of claim 1. Wistron contends that the disclosures identified by Phenix provide only that "[t]he banks of gamma voltages are stored and selected through the three address inputs B0, B1, B2" as well as a programming method that involves selecting a particular cell within a bank to be programmed. Docket No. 104 at 38 (quoting and citing '305 Patent at 5:52–53, 5:60–6:53). Wistron contends that describing the selection process and the inputs through which a particular bank is selected is not the same as disclosing the actual structure that performs the

selection. *Id.* Wistron contends that a POSITA would expect disclosure of, for example, an address decoder, but no such disclosure is present in the specification of the '305 Patent. *Id.*

Wistron contends that the pins are inputs, which are incapable of selecting anything. *Id.* Wistron contends that the box labelled "Bank Select" in Figure 6 is not sufficient to render "means to switch between banks" definite because it is not a disclosure of an actual structural component. Docket No. 104 at 38 (citing *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 518–19 (Fed. Cir. 2012)).

TI notes that its construction is nearly identical to Phenix's construction in the *IML* litigation. Docket No. 104 at 39. TI contends that Phenix's construction lacks two concepts: (1) the use of a damping circuit during switching and (2) that the input pins B0–B2 can also be used during programming of the integrated circuit.

TI points to the '305 Patent as discussing an "internal damping circuit" of the switching mechanism that "creates a slow transition, about 10 msec., between banks." '305 Patent at 5:60–6:21. TI further points to Figure 5 as showing a parameter "Tdamp" that sets the "Bank Switch Damp Time," which is the time between transitions between banks during switching. Docket No. 104 at 40. TI contends that the rapid transitions directly relate to switching because the patent is discussing transitions "between banks." *Id.* (citing '305 Patent at 5:64–66). TI also notes that in both the original Wistron briefing and the *IML* litigation, Phenix identified the '305 Patent's disclosures at column 5, line 50 through column 6, line 21 and Figure 5's Tdamp as part of the "corresponding structure" for this claim element. *Id.* (citing Docket 73 at 25; Docket No. 104-19 (*IML* Brief) at 23). TI also states that Phenix's expert, Mr. Murphy, opined that "means to switch between the banks based on one more external signals" are disclosed in figures including "Fig[ure] 5 ('Bank Switch Damp Time' is 10 msec)" and that "[a] detailed description of the means to switch

between the banks is found in the ’305 Patent’s written description associated with these figures at 5:50–6:22 (FIG. 6).” *Id.* (quoting Docket 104-10 ¶¶ 57–58). Finally, TI notes that after Phenix submitted its opening brief, Phenix represented to the PTAB that “[t]he structure . . . includes an internal damping circuit, which is referred to in Figure 5 as ‘Bank Switch Damp Time.’ ” *Id.* (quoting Docket 104-21 (Patent Owner Preliminary Response) at 18–19).

As to the programming concept, TI contends that ’305 Patent provides detail as to how the input pins B0–B2 are used during the programming process. ’305 Patent at 6:34–53 (“the particular bank is addressed through B0–B2; Vpp is pulsed again, latching the bank address.”); Docket No. 104 at 41.

As to the damping circuitry, Phenix contends that the specification clearly states that such circuitry is optional. ’305 Patent at 5:62–66 (“[***w]hen deemed appropriate*** an internal damping circuit creates a slow transition, about 10 msec., between banks to prevent disruptive display artifacts caused by rapid transitions on the gamma reference voltages during operation.”) (emphasis added). Phenix argues that this damping circuity does not perform the function of “switching between the banks based on one or more external signals” but only slows down what is called the slew rate at the output of the device, depending on the “display manufacturer’s requirements.” Docket No. 106 at 11. Phenix contends that TI is restricting the corresponding structure to a structure disclosed in one embodiment and that is not necessary to perform the recited function of “switching between the banks based on one or more external signals.” *Id.*

Analysis

Wistron argues that the “Bank Select” of Figure 6 is merely a generic functional block diagram; however, the testimony of the experts supports the position that this is circuitry that has been well-known for years. *See* Docket No. 100-13 ¶¶ 87–90; *see* Docket No. 100-8 (Flasck Tr.) at 169:4–17; *see also Teva Pharm.*, 135 S. Ct. at 841. The specification makes clear that the bank

pins and the bank select provide for switching. '305 Patent at 5:50–6:21; Figure 4A (B0–B2); Figure 4B (pins 20, 22, 23); Figure 5 (Tdamp); Figure 6 (Bank Select, B0, B1, B2).

A closer issue is whether the corresponding structure includes the damping circuitry. The only detailed disclosure of bank selection includes the damping circuit concept being used when switching between banks. '305 Patent at 5:60–6:21. However, the specification references the damping feature as being applied "when deemed appropriate." *Id.* This statement may be interpreted in two ways: first, that the disclosed bank select circuitry has damping capability that is used when appropriate and, alternatively, that the addition of damping circuitry is optional. The Court finds that the former interpretation applies here. As presented in the specification, this circuitry is directly related to the switching between banks. In the context of the intrinsic record, the Court finds that the switching structure includes the internal damping circuit.

At the hearing, Phenix argued that the damping would occur at the voltage outputs and not as part of the switching. Docket No. 123 at 111–112, 118–119. When asked where in the specification damping at the output is described, Phenix could not identify any passages. *Id.* at 119–120. The specification, however, describes the use of banks and slowing the transition between banks by damping when switching between banks:

> When deemed appropriate an internal damping circuit creates a slow transition, about 10 msec., between banks to prevent disruptive display artifacts caused by rapid transitions on the gamma reference voltages during operation. Alternative damping circuits may be employed which allow the transition between banks to be considerably slower, for instance, one second, as may be required by the display manufacturer's requirements.

'305 Patent at 5:62–6:21.

Phenix's own expert has twice included the damping circuitry in his construction. Docket 104-10 (Murphy Decl. (Oct. 7, 2018)) ¶¶ 87–88; Docket No. 104-18 (Murphy Decl. (Sept. 12, 2018)) ¶¶ 57–58. Additionally, after Phenix submitted its opening brief, Phenix represented to the

PTAB that "[t]he structure . . . includes an internal damping circuit, which is referred to in Figure 5 as 'Bank Switch Damp Time.' " Docket 104-21 (Patent Owner Preliminary Response) at 18–19. On balance, the record supports inclusion of the damping circuit.

Finally, TI's construction also relies on the '305 Patent's disclosure of the bank select inputs B0–B2. '305 Patent at 6:34–53. Such disclosure makes it clear that the usage of the inputs is described in relation to the programming of a cell. That the pins may additionally be used for other functions does not warrant adding that passage to the switching function. The programming function is a different function than the switching function and the corresponding structure is limited to the structure that performs the referenced function. *See Micro Chem.*, 194 F.3d at 1258.

The Court construes "means to switch between the banks based on one or more external signals" to mean:

Function: switching between the banks based on one or more external signals;

Structure: '305 Patent, 5:50-6:21; Figure. 4A (B0-B2); Figure. 4B (pins 20, 22, 23); Figure. 5 (Tdamp); Figure. 6 (Bank Select, B0, B1, B2).

9. "high voltage programming means" (claim 5)

Phenix	Wistron	TI
Plain and ordinary meaning -------------------------------- Alternatively, the term is written as means-plus-function subject to § 112 ¶ 6 **Function**: high voltage programming of non-volatile storage cells **Structure**: FIG 4A (Vpp); FIG. 4B (pin 2); FIG. 6; the '305 Patent 6:27–31, 45–47	Indefinite	This term is written as a means-plus-function subject to § 112 ¶ 6 **Function**: programming using a high voltage signal **Structure**: '305 Patent, 6:22-67; Fig. 4A (Vpp, Aout, A0–A1, B0–B2); Fig. 4B (Vpp, Aout, A0–A1, B0–B2); Fig. 5 (Vpp); Fig. 6 (Programming Interface, Vpp, Aout, A0–A1, B0–B2)

The term is found in claim 5: "wherein said circuits for programming require an external source for the high voltage programming means." Wistron contends that the specification only discloses using a high voltage signal to program and does not identify corresponding structure for the actual circuitry. Phenix and TI agree the term is definite but dispute whether the structure should include the Aout, A0–A1 and B0–B2 pins.

Positions of the Parties

Phenix asserts that the following specification passage discloses sufficient supporting structure:

> The Vpp is a high voltage input used to select the programming mode and also provides the high voltage pulses used to program individual cells. In the AG1818 embodiment, Vpp is supplied from an external source, an IC or other means.

'305 Patent at 6:27–31. Phenix contends that Figure 4A lists the pins and their functions along with voltage values that are used for programming the chip. Phenix also contends that the patent provides a detailed description of the sequence of events to program the memory ('305 Patent at 6:37–53) and that the key variables in the programming process are taught as varying depending upon the fabrication facility ('305 Patent at 6:54–65). Docket No. 100 at 42.

Phenix argues that TI improperly imports the analog output monitoring voltage pin (Aout), address pins (A0–A1) and bank select pins (B0–B2) as part of a high voltage programming means. Phenix states that while one of the embodiments in the '305 Patent uses the address pins and bank select pins for entering certain program modes, the bank select pins are already recited in claim 1 as the "means to switch between the banks," and the address pins are recited in claim 1 as "wherein the addressing is based on a plurality of inputs." *Id.* at 42–43.

Phenix contends that a POSITA would not understand the Aout pin to be an "external source for a high voltage programming means" because it is an output pin for an output signal used

to measure and verify the voltage in a non-volatile storage cell. *Id.* (citing '305 Patent at 6:58–68). Phenix argues that the selection of the location of memory cells using address pins (A0–A1) and bank select pins (B0–B2) are always from external sources since these signals are generated outside of the integrated circuit; therefore, "external source" is not a limiting design choice for these input signals. Phenix contends that a POSITA would not understand the memory address and bank select structures to be included in the structure for claim 5. According to Phenix, the only signal that can be generated either off-chip or on-chip is the high voltage used to program the non-volatile storage cell, which is known to a POSITA as Vpp. Docket No. 100 at 43. Phenix states that the limitation requiring an "external source" for the high voltage programming means can, thus, only refer to a pin needed to conduct the external signals to the integrated circuit; i.e., the Vpp pin described in the '305 Patent. *Id.*

Phenix further states that its expert, Mr. Murphy, establishes that programing of storage cells with high voltages was well-known in the prior art for years. Phenix also states that Wistron's PTAB expert testified that it was well-known that high voltages were required to program the cells and that such voltages could be provided externally or internally. *Id.* at 43–44. Phenix notes that Wistron and its PTAB expert had no problem interpreting the term in the PTAB proceedings. *Id.* at 44.

Wistron contends that the '305 Patent fails to disclose structure capable of performing "high voltage programming." Docket No. 104 at 41. Wistron states that the '305 Patent describes programming analog storage cells using variable, high voltage programming pulses. Wistron contends, however, that nothing in the '305 Patent discloses the circuits that actually generate those pulses. *Id.* at 42. Wistron states that Phenix merely cites to passages that describe "Vpp" (the electrical signal that carries the programming pulses), rather than circuitry. *Id.* Wistron asserts

that the specification does not describe circuitry or structure, and that the inventors intentionally chose not to disclose any specifics because such algorithms were "trade secrets." *Id.* (citing Docket No. 104-6 (Orlando Tr.) at 139:7–140:9). Wistron contends that the inventors acknowledged that specialized hardware would be needed to generate the high voltage pulses, but none was shown in the patent. *Id.*

TI asserts that, under *Williamson*, the use of "means" creates a presumption that the term is a means-plus-function term. TI contends that Phenix has provided no argument or evidence that the term is not a means-plus-function term. Docket No. 104 at 43.

According to TI, Phenix's proposed function of "high voltage programming of non-volatile storage cells" is unnecessary because the programming of "non-volatile storage cells" is implied by the surrounding claim language.

TI notes that TI and Phenix agree that (1) the Vpp pin is a part of the corresponding structure and (2) the specification "provides a detailed description of the sequence of events to program the memory at 6:37–53" and that "[t]he key variables in the programming process is [sic] taught by the '305 Patent as varying, depending on the fabrication facility, at 6:54–65." Docket No. 104 at 43. TI states the '305 Patent expressly describes the use of Aout, A0–A1 and B0–B2 for high voltage signal programming; however, Phenix disputes that Aout, A0–A1 and B0–B2 are part of a high voltage programming means. Docket No. 104 at 43–44.

TI contends that its construction is supported by its expert, Dr. Baker. TI further states that Phenix's expert, Mr. Murphy, agrees that "[a] detailed description [of] high voltage programming is found in the '305 Patent's written description associated with these figures at 6:22–7:19 (FIG. 6)." *Id.* at 44 (quoting Docket No. 104-10 (Murphy Decl. Oct. 7, 2018) ¶ 64; Docket No. 104-18 (Murphy Decl. Sept. 12, 2018) ¶ 49). TI notes that Mr. Murphy's cite to the '305 Patent (6:22–

7:19) includes Aout, A0–A1 and B0–B2. TI also points out that the specification explains "[t]he programming interface consists of four signals." *Id.* TI states that the four signals include Aout, A0–A1 and B0–B2, as found in TI's construction. *Id.* (citing '305 Patent at 6:27–36). TI also notes that Phenix's position in the *IML* litigation included Aout, A0–A1 and B0–B2. *Id.* (citing Docket No. 104-19 (*IML* Brief) at 24).

TI contends that Phenix's argument that the pins cannot be part of two claim elements is legally erroneous because a single structural element may perform two functions and may also support two different claim terms. *Id.* (citing *Winbond Elecs. Corp. v. Int'l Trade Comm'n*, 4 F. App'x 832, 839–40 (Fed. Cir. 2001) ("a single structure, such as a decoder or a buffer, may support two different claim limitations")).

TI contends that the Vpp pin is one of the four signals that constitutes the programming interface, and when the Vpp signal is connected to an external source, then the programming interface, as a whole, is connected to an external source. *Id.* at 44–45.

In reply, Phenix notes that TI and TI's expert agree that the '305 Patent discloses adequate structure for the high voltage programming means. Docket No. 106 at 12. Phenix contends that its expert and the evidence of Wistron's expert, Dr. Thomas Credelle, both support finding that adequate structure is disclosed. *Id.* As to the overlapping use of pins in multiple claim terms, Phenix contends that just because a structure "may" be included in multiple claim elements does not mandate such inclusion. Phenix contends that the plain language of claim 5 requires "an external source for a high voltage programming means." Phenix states that the only structure needed to conduct external signals to the claimed integrated circuit is the Vpp pin. Phenix contends that TI improperly incorporates structural limitations from the written description that are merely optional and unnecessary to perform high voltage programming. *Id.* at 13.

Analysis

The claim term uses "means," which creates a presumption that the term is a means-plus-function term. *Williamson*, 792 F.3d at 1347–49, 1349 n.3. Phenix has not substantively argued against the presumption. Though the parties provide differing functions, none of the parties established a meaningful difference between the proposed functions. In context of the claim, the Court adopts the function of "programming the non-volatile storage cells using a high voltage signal."

The Court finds that sufficient structure is disclosed in the specification. Phenix would limit the structure to a high voltage Vpp pin; however, it is clear that the function includes programming, which involves more than merely receiving an external high voltage source. With reference to the high voltage programming embodiment (Figures 4A, 4B, 5 and 6), what performs the programming is, at a minimum, the Vpp pin and the programming interface and provision of the Vpp signal to the storage cells. *See* '305 Patent at Figures 4A, 4B, 5, 6, 6:22–23. Moreover, as both Phenix and TI have noted, the '305 Patent provides a detailed discussion of high voltage programming using an external source. *See* '305 Patent at 6:22–36.

The first paragraph of column 6 of the '305 Patent discusses use of the programming interface. '305 Patent at 6:22–23 ("programming interface allows the device to be programmed in-situ."). This paragraph also states that "Vpp is a high voltage input used to select the programming mode and also provides the high voltage pulses used to program the individual cells." *Id.* at 6:27–29. The address and bank pins are also involved. *Id.* at 6:34–36 ("The A0 through A1 inputs are used in conjunction with the B0-B2 inputs to select the location to be written."). Thus, this paragraph (and the accompanying Figure 6) provides an embodiment in which the programming interface is used, the Vpp pin is used to set the programming mode, the

Vpp pin is also used to provide the high voltage pulses and the address and bank pins are used for directing the program pulses to the proper storage cell location. Thus, as described in this first paragraph, circuitry for programming includes the programming interface, Vpp pin and the address and bank pins.

TI further urges the Court to include the Aout pin in its construction. However, as described in the specification, the Aout pin does not program a storage cell. Rather, "[t]he Aout analog output is used to read the cell which is currently being programmed to verify the write operation and proper output voltage level." *Id.* at 6:32–34. Thus, programming may occur even without usage of the Aout pin as that pin is merely used to read a cell and verify a cell's voltage. As such, the Court finds that inclusion of Aout would unnecessarily expand the scope of the corresponding structure.

TI asserts that the corresponding structure further requires the circuitry disclosed in the second paragraph of column 6, lines 37–53. However, the first paragraph alone provides circuitry for performing the claimed function. The second paragraph provides an alternative approach to programming that differs from the description of the first paragraph because the second paragraph provides that "[o]ne alternative method of programming the individual cells starts by placing A0, A1, B0, B1, B2 lines in the (1, 1, 1, 1, 1) state and taking the Vpp pin high; this places the AG1818 in the Program mode." '305 Patent at 6:37–40. In this section, Vpp and the address and bank lines (A0, A1, B0, B1, B2) are all used together to set the program mode. Next, a bank is selected with the bank pins, and a particular cell to be programmed is selected with the address and the bank pins. *Id.* at 6:41–44. Then, the programming is completed by pulsing the Vpp pin. *Id.* at 6:45–47 ("At this point programming of the selected storage cell is initiated by pulsing Vpp with adjustable voltage pulses between approximately 8 and 14 volts.").

The Court's construction reflects the two alternate descriptions of operation of the corresponding structure utilized for programming a storage cell as described above.

The Court construes "high voltage programming means" to mean:

Function: programming the non-volatile storage cells using a high voltage signal;

Structure:

(1) (a) a Program Interface, (b) a Vpp input that is used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an individual cell, and (d) address inputs A0 and A1 / bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:22-36, Figure 4A, Figure 4B, Figure 5 and Figure 6

and/or

(2) (a) a Program interface, (b) a Vpp input, address inputs A0 and A1, and bank inputs B0, B1, B2 that are used to select the programming mode, (c) the Vpp input also providing the high voltage pulses used during programming of an the individual cell, and (d) address inputs A0 and A1 and bank inputs B0, B1, B2 used to select the location being programmed; as described at '305 Patent 6:37-53, Figure 4A, Figure 4B, Figure 5 and Figure 6

CONCLUSION

The Court adopts the constructions above for the disputed and agreed terms of the '305 Patent. Furthermore, the parties should ensure that all testimony that relates to the terms addressed in this Order is constrained by the Court's reasoning. However, in the presence of the jury the parties should not expressly or implicitly refer to each other's claim construction positions and should not expressly refer to any portion of this Order that is not an actual construction adopted by the Court. The references to the claim construction process should be limited to informing the jury of the constructions adopted by the Court.

IT IS SO ORDERED.

So ORDERED and SIGNED this 21st day of June, 2019.

Robert W Schroeder III

ROBERT W. SCHROEDER III
UNITED STATES DISTRICT JUDGE